05-07-01

EL465779847US

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JC984 U.S. PTO

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PTO/SB/05 (4/98)
Approved for use through 09/30/2000 OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C F.R § 1.53(b))

Attorney Docket No.	MI22-1689
First Inventor or Application Identifier	Luan C. Tran
Title	Semiconductor Processing Methods etc.
Express Mail Label No.	EL465779847US

J1033 U.S. PTO 09/847880 05/03/01

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 29] Plus title pg.
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 4]
4. Oath or Declaration [Total Pages 2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

*** NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).**

5. [ ] Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [X] Assoc. Power of Attorney
9. [ ] English Translation Document (if applicable)
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
13. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
15. [X] Other: Sub. Drawing Request
    Sub. Formal Drawings

16. If a **CONTINUING APPLICATION**, check appropriate box, and supply the requisite information below and in a preliminary amendment:
[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No 09 / 388,856
Prior application information: Examiner L. Schillinger Group / Art Unit: 2813

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label 021567 (Insert Customer No. or Attach bar code label here) or [X] Correspondence address below

Name	Frederick M. Fliegel, Ph.D. Wells, St. John, Roberts, Gregory & Matkin P.S.				
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Name (Print/Type)	Frederick M. Fliegel, Ph.D.	Registration No (Attorney/Agent)	36,138
Signature	[signature]	Date	May 3, 2001

Burden Hour Statement This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

EL465779847

PTO/SB/17 (11-00)
Approved for use through 10/31/2002. OMB 0651-0032
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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1,130.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Luan C. Tran
Examiner Name	
Group Art Unit	
Attorney Docket No.	MI22-1689

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to

Deposit Account Number: 23-0925

Deposit Account Name: Wells, St. John et al.

[X] Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17

[ ] Applicant claims small entity status See 37 CFR 1 27

2. [X] **Payment Enclosed:**

[X] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	710
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	30	-20** =	10	x	18	=	180
Independent Claims	6	- 3** =	3	x	80	=	240
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 420.00

***or number previously paid, if greater, For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1 17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1 129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ______

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 0

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Frederick M. Fliegel, PhD	Registration No (Attorney/Agent)	36,138	Telephone	509-624-4276
Signature	[signature]			Date	May 3, 2001

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U S Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Washington, DC 20231

EL465779847

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/388,856
Priority Filing Date . . . . September 1, 1999
Inventor . . . . Luan C. Tran
Assignee . . . . Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner . . . . L. Schillinger
Attorney's Docket No. MI22-1689
TITLE: Semiconductor Processing Methods of Forming Integrated Circuitry

Assistant Commissioner for Patents
Washington, D. C. 20231
Attention: Official Draftsman

SUBSTITUTE DRAWING REQUEST

Please enter the enclosed substitute drawings in the above-referenced application in place of drawings originally filed. The content of the drawings are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawings and their acceptance into the file is requested.

Respectfully submitted,

Date: May 3, 2001

By: [signature]

Frederick M. Fliegel, Ph.D.
Reg. No.: 36,138
WELLS, ST. JOHN, ROBERTS,
GREGORY & MATKIN P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276

Enclosures: 4 Sheets of Formal Drawings, Figs. 1-7.

EL465779847

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<u>Priority</u> Application Serial No. 09/388,856
<u>Priority</u> Filing Date ....September 1, 1999
Inventor ....Luan C. Tran
Assignee.. Micron Technology, Inc.
<u>Priority</u> Group Art Unit 2813
<u>Priority</u> Examiner ....L. Schillinger
Attorney's Docket No. MI22-1689
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
Tel. 509-624-4276; Fax 509-838-3424
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817

Sir:

This is a preliminary amendment accompanying a Request for Divisional Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

At page 1, after the title insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/388,856, filed on September 1, 1999, entitled "Semiconductor Processing Methods of Forming Integrated Circuitry" and naming Luan C. Tran as inventor.

In the Claims

Please cancel claims 18-36 without prejudice.

Please amend claims 5, 16 and 45 as follows:

1. A semiconductor processing method of forming integrated circuitry comprising:

forming memory circuitry and peripheral circuitry over a substrate, the peripheral circuitry comprising first and second type MOS transistors; and

conducting second type halo implants into the first type MOS transistors in less than all peripheral MOS transistors of the first type.

2. The semiconductor processing method of claim 1, wherein the second type is p-type.

3. The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

4. The semiconductor processing method of claim 1, wherein:

the second type is p-type; and

the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

5. (Amended) A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

6. The method of claim 5, wherein said three devices comprise peripheral circuitry.

7. The method of claim 5, wherein said three devices comprise NMOS field effect transistors.

8. The method of claim 5, wherein said three devices comprise NMOS field effect transistors comprising peripheral circuitry.

9. The method of claim 5, wherein said three devices comprise PMOS field effect transistors.

10. The method of claim 5, wherein said three devices comprise PMOS field effect transistors comprising peripheral circuitry.

11. The method of claim 5, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices.

12. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

13. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

14. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

15. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

16. (Amended) A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, at least some of the devices forming memory access devices.

17. The method of claim 16, wherein the at least some of the devices forming memory access devices receive halo implants on a bitline contact side of the devices.

Claims 18-36 have been canceled without prejudice.

37. A semiconductor processing method of forming integrated circuitry comprising:

forming a plurality of NMOS field effect transistor devices over a substrate comprising memory array circuitry and peripheral circuitry, individual NMOS transistor devices having source regions and drain regions;

forming a mask over the substrate, the mask (a) exposing source and drain regions of first NMOS transistor devices, (b) covering source and drain regions of second NMOS transistor devices, and (c) partially exposing only a portion of third NMOS transistor devices; and

with the mask in place, conducting a halo implant.

38. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing an entirety of one of the source and drain regions and not an entirety of the other of the source and drain regions for the third NMOS transistor devices.

39. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing one of the source and drain regions and not the other of the source and drain regions for the third NMOS transistor devices.

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40. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing a portion of one of the source and drain regions and not the other of the source and drain regions for the third NMOS transistor devices.

41. A method of improving DRAM storage cell retention time comprising conducting, in a common masking step and in a common implant step, a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to each device one of two or more different respective threshold voltages, at least some of the devices forming memory access devices, wherein the at least some of the devices forming memory access devices receive halo implants on a bit line contact side of the devices.

42. The method of claim 41 wherein the halo implant is performed prior to formation of sidewall spacers in the memory access devices.

43. The method of claim 41 wherein the halo implant is performed after formation of sidewall spacers in the memory access devices.

44. The method of claim 41 wherein the halo implant is accompanied with an n-minus implant on the bit line contact side.

45. (Amended) The method of claim 41 wherein the storage node side of the memory access device is masked from the halo implant.

46. A method of improving DRAM storage cell retention time comprising forming memory access devices having different implants and hence different junction structures on a bitline contact side and a storage node side respectively.

47. The method of claim 46 wherein forming memory access devices includes:

performing, during a masking and implant step, a one-sided halo implant on the bitline contact side; and

performing, during the masking and implant step, an n-minus implant on the bitline contact side.

48. The method of claim 47, wherein performing a one-sided halo implant is performed prior to formation of sidewall spacers.

49. The method of claim 46, wherein the storage node side is masked during a one-sided halo implant on the bitline contact side.

REMARKS

This application is a divisional application of U.S. Patent Application Serial No. 09/388,856 and is being filed responsive to a restriction requirement therein. Accordingly, claims 18-36 have been canceled without prejudice. Claims 1-17 and 37-49 remain in the application for consideration.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: May 3, 2001

By: [signature]
Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

09/847,865 - 050301

Version with markings to show changes made.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/388,856
Priority Filing Date ....September 1, 1999
Inventor ....Luan C. Tran
Assignee... Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner ....L. Schillinger
Attorney's Docket No. MI22-1689
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

At page 1, after the title insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/388,856, filed on September 1, 1999, entitled "Semiconductor Processing Methods of Forming Integrated Circuitry" and naming Luan C. Tran as inventor.

In the Claims

Claims 18-36 have been canceled without prejudice.

Claims 5, 16 and 45 have been amended as shown below.

5. (Amended) [In a common] A semiconductor processing method comprising:

a masking step providing a common mask; and [in]

[a common] an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

16. (Amended) [In a common] A semiconductor processing method comprising:

a [common] masking step providing a common mask; and [in]

[a common] an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, at least some of the devices forming memory access devices.

45. (Amended) The method [ov] of claim 41 wherein the storage node side of the memory access device is masked from the halo implant.

END OF DOCUMENT

EL366000035

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Semiconductor Processing Methods Of Forming Integrated Circuitry

* * * * *

INVENTOR

Luan C. Tran

ATTORNEY'S DOCKET NO. MI22-982

SEMICONDUCTOR PROCESSING METHODS OF FORMING INTEGRATED CIRCUITRY

TECHNICAL FIELD

This invention relates generally to semiconductor processing methods of forming integrated circuitry, and particularly to methods of forming integrated circuit devices having different threshold voltages.

BACKGROUND OF THE INVENTION

Field effect transistors are characterized by a source region, a drain region and a gate. The source and drain regions are typically received within a semiconductive material, such as a semiconductive substrate. The gate is typically disposed elevationally over the source and drain regions. A gate voltage of sufficient minimum magnitude can be placed on the gate to induce a channel region underneath the gate and between the source and drain regions. Such channel-inducing voltage is typically referred to as the transistor's threshold voltage, or V_t. Accordingly, the threshold voltage turns the transistor on. Once the magnitude of the threshold voltage has been exceeded, current can flow between the source and drain regions in accordance with a voltage called the source/drain voltage, or V_{ds}.

Threshold voltage magnitudes can be affected by channel implants. Specifically, during fabrication of semiconductor devices, a substrate can be implanted with certain types of impurity to modify or change the

threshold voltage of a resultant device. Such channel implants can also affect a condition known as subsurface punchthrough. Punchthrough is a phenomenon which is associated with a merging of the source and drain depletion regions within a MOSFET. Specifically, as the channel gets shorter (as device dimensions get smaller), depletion region edges get closer together. When the channel length is decreased to roughly the sum of the two junction depletion widths, punchthrough is established. Punchthrough is an undesired effect in MOSFETS.

One way of addressing punchthrough in sub-micron devices is through provision of a so-called halo implant, also known as a "pocket" implant. Halo implants are formed by implanting dopants (opposite in type to that of the source and drain) within the substrate proximate the source and drain regions, and are typically disposed underneath the channel region. The implanted halo dopant raises the doping concentration only on the inside walls of the source/drain junctions, so that the channel length can be decreased without needing to use a higher doped substrate. That is, punchthrough does not set in until a shorter channel length because of the halo.

It is desirable to have MOSFETS with different threshold voltages depending upon the context in which the integrated circuitry of which they comprise a part is to be used. In the context of memory devices it can be beneficial to have transistors with different threshold voltages.

This invention arose out of concerns associated with improving the methods through which integrated circuits are fabricated. In particular, the invention arose concerns associated with providing improved methods of forming memory devices.

SUMMARY OF THE INVENTION

Semiconductor processing methods of forming integrated circuitry are described. In one embodiment, memory circuitry and peripheral circuitry are formed over a substrate. The peripheral circuitry comprises first and second type MOS transistors. Second type halo implants are conducted into the first type MOS transistors in less than all of the peripheral MOS transistors of the first type. In another embodiment, a plurality of n-type transistor devices are formed over a substrate and comprise memory array circuitry and peripheral circuitry. At least some of the individual peripheral circuitry n-type transistor devices are partially masked, and a halo implant is conducted for unmasked portions of the partially masked peripheral circuitry n-type transistor devices. In yet another embodiment, at least a portion of only one of the source and drain regions is masked, and at least a portion of the other of the source and drains regions is exposed for at least some of the peripheral circuitry n-type transistor devices. A halo implant is conducted relative to the exposed portions of the source and drain regions. In another embodiment, a common masking step is used and a halo implant is

conducted of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer fragment in process, which is suitable for use in connection with one or more embodiments of the present invention.

Fig. 2 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 3 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 4 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 5 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 6 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 7 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment in process is shown generally at 10 and includes a semiconductive substrate 12. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Memory array circuitry 14 and peripheral circuitry 16 are formed over substrate 12. Memory circuitry 14 comprises individual transistors 20, 22. Peripheral circuitry 16 comprises a transistor 26. These transistors are shown for example only. Each exemplary transistor will typically include a conductive gate line 28 (designated for transistors 20 and 26 only) having a gate oxide layer 30, a polysilicon layer 32, a silicide layer 34, and an overlying insulative cap 36. Conventional sidewall spacers SS are optionally provided over the sidewalls of gate

line 28. Of course, other gate line constructions could be used. Source/drain regions 37 and 38 are provided within substrate 12.

The drain regions 37 may be formed in several different ways. In one embodiment, the drain regions 37 are doped first with a blanket n-minus implant, which may be performed before or after formation of the sidewalls SS. As used herein, the term "blanket implant" refers to an implant process that does not employ a masking step. In one embodiment, the drain regions 37 are doped by out-diffusion of dopants from a doped polysilicon layer forming a portion of a storage node 39.

The source regions 38 may also be formed in several different ways. In one embodiment, the source regions are doped first with a blanket n-minus implant 37' and then with a n-plus implant, followed by a halo implant 41.

Typically, the transistors forming peripheral circuitry 16 will include first- and second-type MOS transistors. For example and for purposes of the on-going discussion, first-type MOS transistors will comprise n-type transistors, and second-type MOS transistors will comprise p-type transistors. Similarly, in this example, implants comprising a second-type of material will comprise p-type implants such as boron.

Referring to Fig. 2 and 3, a masking layer 40 is formed over substrate 12. Transistor 42 (Fig. 2) can constitute a transistor which is disposed within the memory array, or one which is disposed within the peripheral area. Similarly, transistor 26 (Fig. 3) can constitute a

transistor which is disposed within the memory array, or one which is disposed within the peripheral area. Transistor 26 can represent one of many similar partially-masked transistors in either the peripheral area or the memory array. In one embodiment, and with masking layer 40 in place, a second-type halo implant is conducted into transistor 26 and in less than all transistors of the first type. The halo implant forms a halo region 41 received within substrate 12. In this case, transistor 42 can constitute a transistor which does not receive the halo implant. In one embodiment, when transistors receive the halo implant, only one side of the transistor receives the implant, such as shown in Fig. 3. This constitutes a different transistor having a different threshold voltage V_t than those transistors not receiving the halo implant.

Specifically, in one embodiment, transistor 26 comprises an n-type transistor device which is partially masked, and the halo implant is conducted for unmasked portions of the transistor or transistors. Various portions of transistor 26 can be masked to result in a partially masked transistor. For example, at least a portion of one of the source and drain regions can be masked, and at least a portion of the other of the source and drain regions can be exposed. As a further example, a majority portion of one of the drain regions can be masked, while a majority portion of the other of the source regions is not masked for at least some of the devices. In the illustrated example, an entirety of one of the drain regions is masked, and the entirety of the other of the

source regions is not masked. Where a transistor's source region is masked, after the halo implantation, the transistor will have a configuration similar to a source follower configuration. Where a transistor's drain region is masked, after the halo implantation, the transistor can have its electric field suppressed proximate the drain.

In another embodiment, the second-type halo implants are conducted into only one of the source and drain regions in less than all of the MOS transistors of the first type, and not the other of the source and drain regions of those peripheral MOS transistors of the first type.

Referring to Fig. 4, another embodiment of the invention is shown. Leftmost transistor 26 can comprise any of the partially-masked configurations described with respect to Fig. 3. Rightmost transistor 26a has both source and drain regions masked, and constitutes other n-type transistor devices which do not receive a halo implant. As a result, the rightmost transistor 26a has a lower threshold voltage V_t than transistors receiving the halo implant.

Referring to Fig. 5, another embodiment of the invention is shown. Leftmost transistor 26 can comprise any of the partially-masked configurations described with respect to Fig. 3. Transistor 26b has both of its source and drain regions left exposed during the halo implant. Accordingly, halo regions 41 are formed proximate the source/drain regions of transistor 26b.

Referring to Fig. 6, another embodiment of the invention is shown. Leftmost transistor 26 can comprise any of the partially-masked configurations described with respect to Fig. 3. In this embodiment, portions of transistors in either the peripheral or the memory array region are partially masked, and, in addition, the source regions and drain regions for some other individual transistor devices are masked, e.g. transistor 26a, while different other individual peripheral transistor devices, e.g. transistor 26b, have their source regions and drain regions exposed during the halo implant. Accordingly, where both of the source and drain regions are exposed, a pair of halo regions 41 is formed. These associated transistor devices having both source and drain regions exposed are, for purposes of this document, referred to as first transistor devices. Where both of the source and drain regions are masked or otherwise blocked, no halo regions are formed. These associated transistor devices having both source and drain regions masked or blocked are, for purposes of this document, referred to as second transistor devices. Where a portion of a transistor device is exposed, a halo region can, in some instances, be formed with respect to only one of the source and drain regions. These associated transistor devices are, for purposes of this document, referred to as third transistor devices. Preferably, these associated transistor devices are all NMOS transistor devices.

Alternately considered, and in a preferred embodiment, a common masking step is utilized and in a common implant step, a halo implant is conducted of devices formed over a substrate comprising memory circuitry and peripheral circuitry, sufficient to impart to at least three of the devices three different respective threshold voltages. In one embodiment, the three devices comprise NMOS field effect transistors.

In the context of NMOS field effect transistors in which the implanted halo impurity comprises a p-type impurity, those transistors whose source and drain regions are fully exposed, will typically have the highest threshold voltage V_{t1}. Those transistors which are partially masked during the halo implant will typically have a threshold voltage V_{t2} which is somewhat lower than threshold voltage V_{t1}. Those transistors whose source and drain regions are completely blocked during the halo implant will typically have the lowest threshold voltage V_{t3} of the threshold voltages. Accordingly, three different threshold voltages are provided through one common masking step.

Fig. 7 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention. Transistors 20 and 22 of Fig. 1 now form memory access transistors 45 having a threshold voltage that corresponds to a single halo implant 41 on a bitline contact side of the access transistors 45. Storage node sides 47 of the access transistors 45 are masked by the masking layer 40 to prevent boron from being implanted. Forming access transistors

45 in this way improves refresh capabilities. The one-sided halo implant 41 in the access transistors 45 allows the channel doping to be reduced while maintaining the same threshold voltage V_t and subthreshold voltage. The lower channel doping, in turn, gives rise to improved DRAM refresh characteristics, because charge leakage from the storage nodes 47 is reduced.

It will be appreciated that the halo implant and the mask 40 therefor may be effectuated before formation of sidewall spacers (denoted "SS" in Fig. 1), as shown in Figs. 2-7, or after formation of sidewall spacers (as shown in Fig. 1). The sidewall spacers SS shown in Fig. 1 may be formed using conventional deposition, oxidation and/or etching techniques. It will be appreciated that when boron is implanted into a n-type device, n-well bias plugs and other conventional features should be masked to avoid compromise of the conductivity of these features.

When the halo implant is done with a mask, prior to formation of sidewall spacers SS, it is normally accompanied by an n-minus implant 37, using either phosphorous or arsenic. When the halo implant is done after formation of the sidewall spacers SS, it is assumed that the n-minus layer 37 was formed earlier as part of a LDD (lightly doped drain) structure. This same halo implant is normally accompanied by an n+ source drain implantation.

One preferred application for such devices can be in the context of peripheral circuitry comprising a so-called equilibrating device, which is typically connected between bit lines D and D* in dynamic random access memory circuitry in order to bring the bit lines to a common voltage potential (typically $V_{cc}/2$) prior to firing the word lines to perform a sensing operation. Another application can be for the cross-coupled transistors in a sense amplifier circuit, where lower threshold voltage V_t is preferred for better margin and refresh properties. Other applications can include various low-voltage applications which will be apparent to the skilled artisan.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

<u>CLAIMS</u>:

1. A semiconductor processing method of forming integrated circuitry comprising:

forming memory circuitry and peripheral circuitry over a substrate, the peripheral circuitry comprising first and second type MOS transistors; and

conducting second type halo implants into the first type MOS transistors in less than all peripheral MOS transistors of the first type.

2. The semiconductor processing method of claim 1, wherein the second type is p-type.

3. The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

4. The semiconductor processing method of claim 1, wherein:

the second type is p-type; and

the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

5. In a common masking step and in a common implant step, conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

6. The method of claim 5, wherein said three devices comprise peripheral circuitry.

7. The method of claim 5, wherein said three devices comprise NMOS field effect transistors.

8. The method of claim 5, wherein said three devices comprise NMOS field effect transistors comprising peripheral circuitry.

9. The method of claim 5, wherein said three devices comprise PMOS field effect transistors.

10. The method of claim 5, wherein said three devices comprise PMOS field effect transistors comprising peripheral circuitry.

11. The method of claim 5, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices.

12. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

13. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

14. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

15. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

16. In a common masking step and in a common implant step, conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, at least some of the devices forming memory access devices.

17. The method of claim 16, wherein the at least some of the devices forming memory access devices receive halo implants on a bitline contact side of the devices.

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18. A semiconductor processing method of forming integrated circuitry comprising:

forming a plurality of n-type transistor devices over a substrate, said n-type devices comprising memory array circuitry and peripheral circuitry, individual n-type transistor devices having source regions and drain regions;

partially masking at least some individual memory array devices and peripheral circuitry n-type transistor devices; and

with said at least some of the memory array and peripheral circuitry n-type transistor devices being partially masked, conducting a halo implant for unmasked portions of said at least some peripheral circuitry n-type transistor devices.

19. The semiconductor processing method of claim 18, wherein the masking comprises masking storage node portions of one of the source region and drain region and not bitline contact portions of the other of the source region and drain region for said at least some individual memory array circuitry n-type transistor devices.

20. The semiconductor processing method of claim 18, wherein the masking comprises masking majority portions of one of the source region and drain region and not majority portions of the other of the source region and drain region for said at least some individual peripheral circuitry n-type transistor devices.

21. The semiconductor processing method of claim 18, wherein the masking comprises masking one of the source region and drain region and not the other of the source region and drain region for said at least some individual peripheral circuitry n-type transistor devices.

22. The semiconductor processing method of claim 18, wherein the masking comprises masking the source regions of said at least some individual peripheral circuitry n-type transistor devices.

23. The semiconductor processing method of claim 18, wherein the masking comprises masking the drain regions of said at least some individual peripheral circuitry n-type transistor devices.

24. The semiconductor processing method of claim 18, wherein the masking comprises (a) masking portions of only one of the source region and drain region for some of the at least some individual peripheral circuitry n-type transistor devices, and also (b) masking both source regions and drain regions for other individual peripheral circuitry n-type transistor devices.

25. The semiconductor processing method of claim 24, wherein said masking of the portions of only one of the source region and drain region comprises masking an entirety of said portions of only one of the source region and drain region for said at least some individual peripheral circuitry n-type transistor devices.

26. The semiconductor processing method of claim 18, wherein the masking comprises (a) masking portions of only one of the source region and drain region for some of the at least some individual peripheral circuitry n-type transistor devices, and also (b) leaving source regions and drain regions exposed for other individual peripheral circuitry n-type transistor devices.

27. The semiconductor processing method of claim 18, wherein the masking comprises (a) masking portions of only one of the source region and drain region for some of the at least some individual peripheral circuitry n-type transistor devices, and also (b) masking both source regions and drain regions for other individual peripheral circuitry n-type transistor devices, and (c) leaving source regions and drain regions exposed for different other individual peripheral circuitry n-type transistor devices.

28. A semiconductor processing method of forming integrated circuitry comprising:

forming a plurality of n-type transistor devices over a substrate comprising memory array circuitry and peripheral circuitry, individual n-type transistor devices having source regions and drain regions;

masking at least a portion of one of the source and drain regions for at least some of the peripheral circuitry n-type transistor devices, and exposing at least a portion of the other of the source and drain regions for said at least some peripheral circuitry n-type transistor devices; and

conducting a halo implant of the exposed portions of the other of the source and drain regions.

29. The semiconductor processing method of claim 28, wherein the masking comprises masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices.

30. The semiconductor processing method of claim 28, wherein the masking comprises exposing the entire portion of the other of said source and drain regions for said at least some peripheral circuitry n-type transistor devices.

31. The semiconductor processing method of claim 28, wherein the masking comprises:

masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices; and

exposing the entire portion of the other of said source and drain regions for said at least some peripheral circuitry n-type transistor devices.

32. The semiconductor processing method of claim 28, wherein the masking comprises also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices.

33. The semiconductor processing method of claim 28, wherein the masking comprises leaving both source regions and drain regions for other peripheral circuitry n-type transistor devices exposed.

34. The semiconductor processing method of claim 28, wherein the masking comprises:

also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices; and

leaving both source regions and drain regions for different other peripheral circuitry n-type transistor devices exposed.

35. The semiconductor processing method of claim 28, wherein the masking comprises:

masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices;

also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices; and

leaving both source regions and drain regions for different other peripheral circuitry n-type transistor devices exposed.

36. The semiconductor processing method of claim 28, wherein the masking comprises:

masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices;

exposing the entire portion of the other of said source and drain regions for said at least some peripheral circuitry n-type transistor devices;

also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices; and

leaving both source regions and drain regions for different other peripheral circuitry n-type transistor devices exposed.

37. A semiconductor processing method of forming integrated circuitry comprising:

forming a plurality of NMOS field effect transistor devices over a substrate comprising memory array circuitry and peripheral circuitry, individual NMOS transistor devices having source regions and drain regions;

forming a mask over the substrate, the mask (a) exposing source and drain regions of first NMOS transistor devices, (b) covering source and drain regions of second NMOS transistor devices, and (c) partially exposing only a portion of third NMOS transistor devices; and

with the mask in place, conducting a halo implant.

38. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing an entirety of one of the source and drain regions and not an entirety of the other of the source and drain regions for the third NMOS transistor devices.

39. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing one of the source and drain regions and not the other of the source and drain regions for the third NMOS transistor devices.

40. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing a portion of one of the source and drain regions and not the other of the source and drain regions for the third NMOS transistor devices.

41. A method of improving DRAM storage cell retention time comprising conducting, in a common masking step and in a common implant step, a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to each device one of two or more different respective threshold voltages, at least some of the devices forming memory access devices, wherein the at least some of the devices forming memory access devices receive halo implants on a bit line contact side of the devices.

42. The method of claim 41 wherein the halo implant is performed prior to formation of sidewall spacers in the memory access devices.

43. The method of claim 41 wherein the halo implant is performed after formation of sidewall spacers in the memory access devices.

44. The method of claim 41 wherein the halo implant is accompanied with an n-minus implant on the bit line contact side.

45. The method ov claim 41 wherein the storage node side of the memory access device is masked from the halo implant.

46. A method of improving DRAM storage cell retention time comprising forming memory access devices having different implants and hence different junction structures on a bitline contact side and a storage node side respectively.

47. The method of claim 46 wherein forming memory access devices includes:

performing, during a masking and implant step, a one-sided halo implant on the bitline contact side; and

performing, during the masking and implant step, an n-minus implant on the bitline contact side.

48. The method of claim 47, wherein performing a one-sided halo implant is performed prior to formation of sidewall spacers.

49. The method of claim 46, wherein the storage node side is masked during a one-sided halo implant on the bitline contact side.

ABSTRACT OF THE DISCLOSURE

Semiconductor processing methods of forming integrated circuitry are described. In one embodiment, memory circuitry and peripheral circuitry are formed over a substrate. The peripheral circuitry comprises first and second type MOS transistors. Second type halo implants are conducted into the first type MOS transistors in less than all of the peripheral MOS transistors of the first type. In another embodiment, a plurality of n-type transistor devices are formed over a substrate and comprise memory array circuitry and peripheral circuitry. At least some of the individual peripheral circuitry n-type transistor devices are partially masked, and a halo implant is conducted for unmasked portions of the partially masked peripheral circuitry n-type transistor devices. In yet another embodiment, at least a portion of only one of the source and drain regions is masked, and at least a portion of the other of the source and drains regions is exposed for at least some of the peripheral circuitry n-type transistor devices. A halo implant is conducted relative to the exposed portions of the source and drain regions. In another embodiment, a common masking step is used and a halo implant is conducted of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

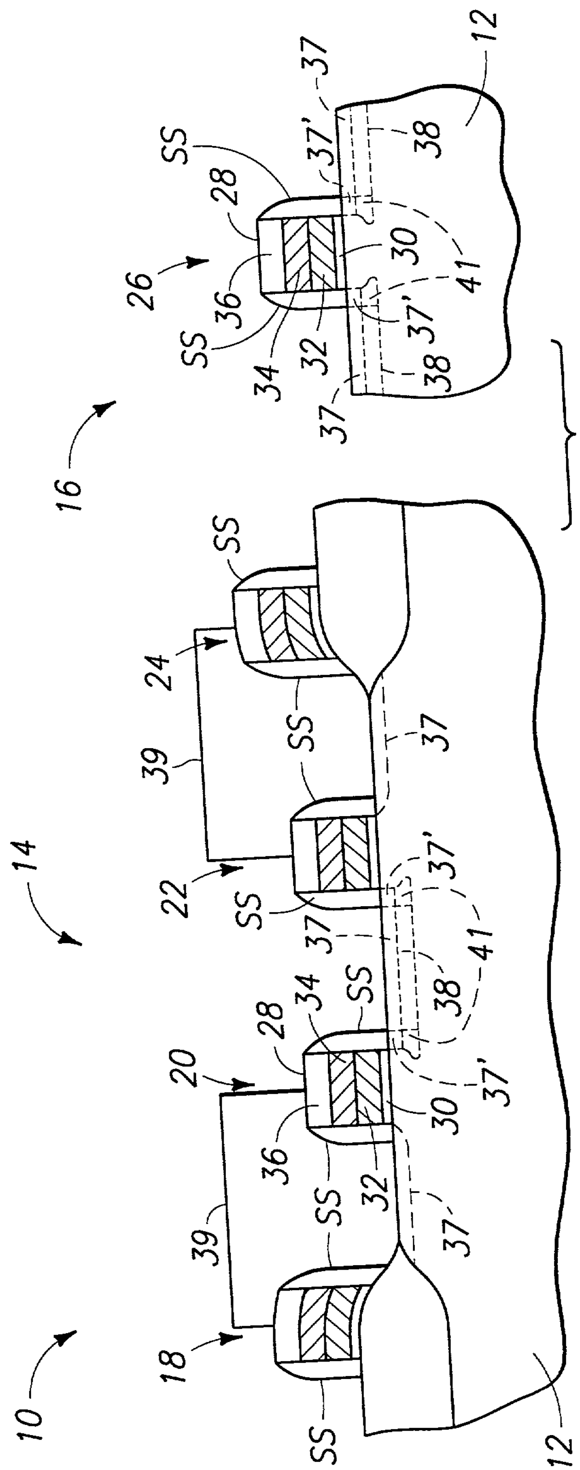

Fig. 1

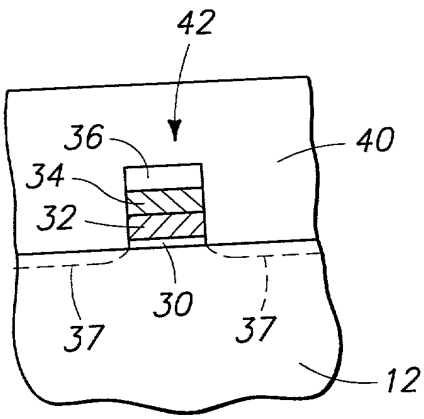

FIG 2

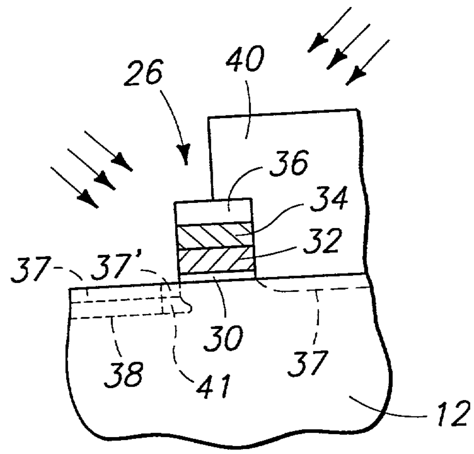

FIG 3

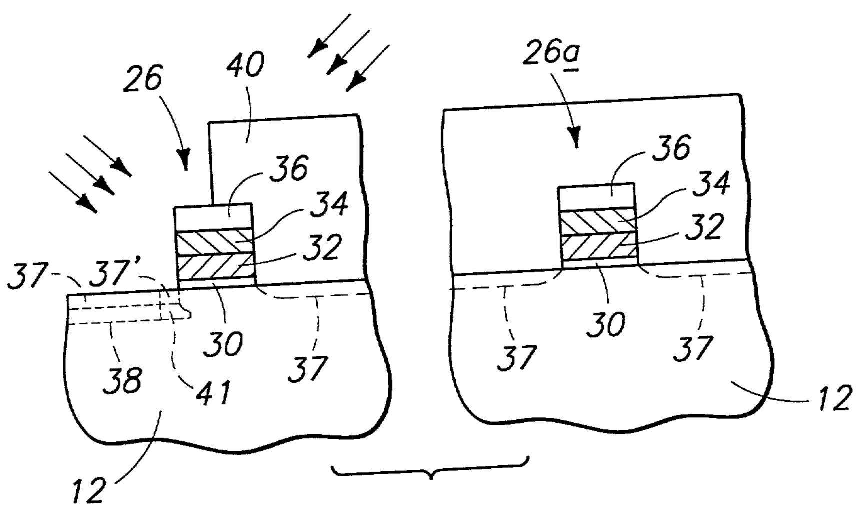

FIG 4

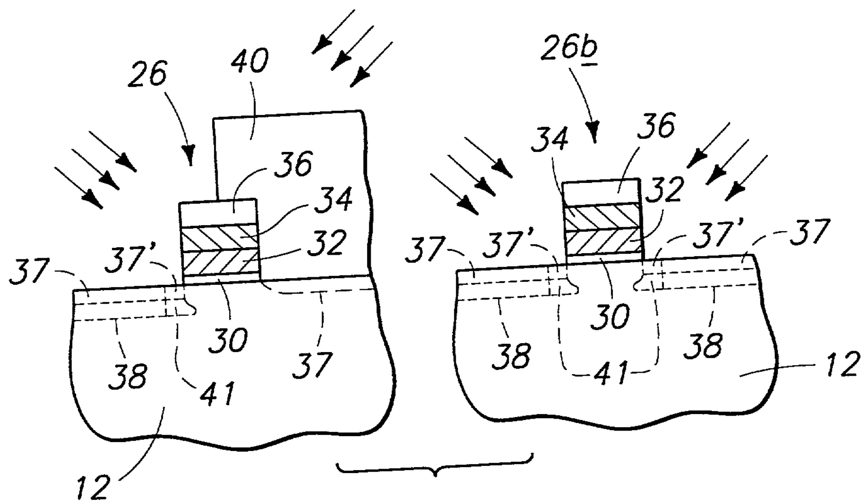
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Fig 5

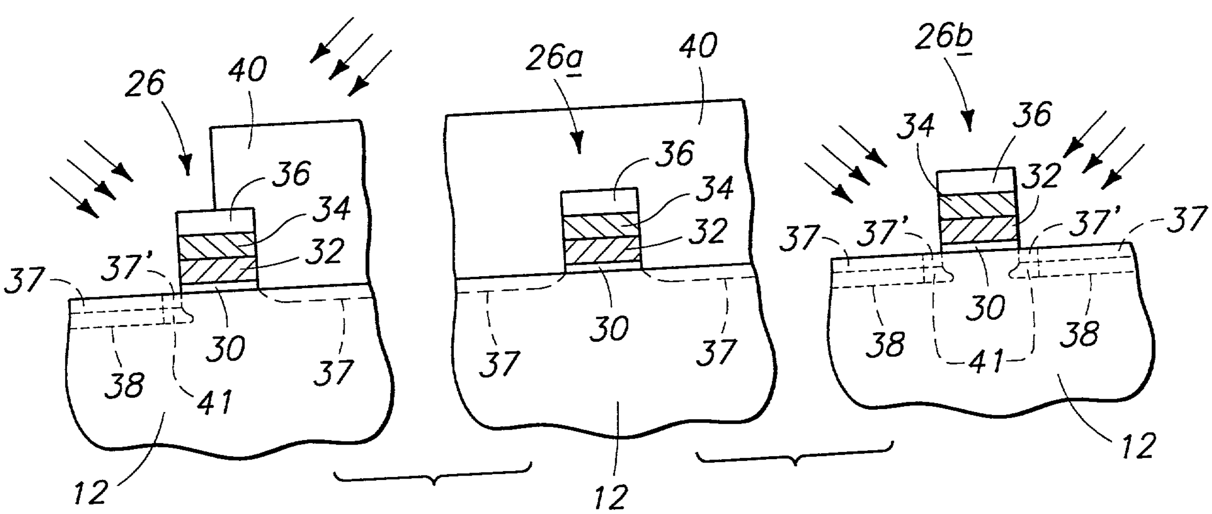
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Fig 6

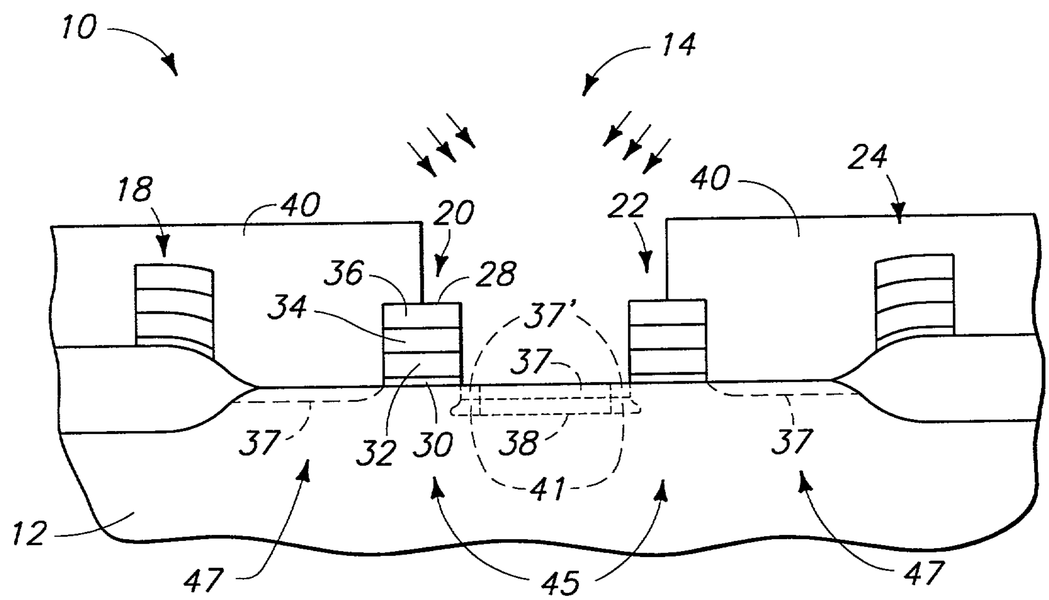

Fig 7

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DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Semiconductor Processing Methods of Forming Integrated Circuitry, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

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* * * * * * * * * * *

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Assignee .... Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner .... L. Schillinger
Attorney's Docket No. MI22-1689
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

Assistant Commissioner for Patents
Washington, D.C. 20231

ASSOCIATE POWER OF ATTORNEY

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